CMOS LINEAR

JANUARY 1989

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1. Life support devices to systems are devices or systems which, are intended for surgical implant into the body to support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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INTRODUCTION

SGS-THOMSON Microelectronics can now offer you a complete range of CMOS LINEAR devices including

— OPERATIONAL AMPLIFIERS

— COMPARATORS

— TIMERS*

This family of monolithic CMOS circuits provides the designers with high performance operation at low supply current and very good speed to power ratio.

* To be introduced 2H89

ALPHANUMERICAL INDEX

PRODUCT GUIDE

LINEAR CMOS

COMPETITION	SGS-THOMSON
TLC271ACD	TS271ACD
TLC271ACP	TS271ACN
TLC271AID	TS271AID
TLC271AIP	TS271AIN
TLC271BCD	TS271BCD
TLC271BCP	TS271BCN
TLC271BID	TS271BID
TLC271BIP	TS271BIN
TLC271CD	TS271CD
TLC271CP	TS271CN
TLC2711D	TS2711D
TLC271IP	TS271IN
TLC272ACD	TS272ACD
TLC272ACP	TS272ACN
TLC272AID	TS272AID
TLC272AIP	TS272AIN
TLC272BCD	TS272BCD
TLC272BCP	TS272BCN
TLC272BID	TS272BID
TLC272BIP	TS272BIN
TLC272CD	TS272CD
TLC272CP	TS272CN
TLC272ID	TS272ID
TLC272IP	TS272IN
TLC274ACD	TS274ACD
TLC274ACN	TS274ACN
TLC274AID	TS274AID
TLC274AIN	TS274AIN
TLC274BCD	TS274BCD
TLC274BCN	TS274BCN
TLC274BID	TS274BID
TLC274BIN	TS274BIN
TLC274CD	TS274CD
TLC274CN	TS274CN
TLC274ID	TS274ID
TLC274IN	TS274IN
TLC27L2ACD	TS27L2ACD
TLC27L2ACP	TS27L2ACN
TLC27L2AID	TS27L2AID
TLC27L2AIP	TS27L2AIN
TLC27L2BCP	TS27L2BCD
TLC27L2BCP	TS27L2BCN
TLC27L2BID	TS27L2BID
TLC27L2BIP	TS27L2BIN
TLC27L2CD	TS27L2CD
TLC27L2CP	TS27L2CN

COMPETITION	SGS-THOMSON
TLC27L2ID	TS27L2ID
TLC27L2IP	TS27L2IN
TLC27L1ACD	TS27L1ACD
TLC27L4ACN	TS27L4ACN
TLC27L4AID	TS27L4AID
TLC27L4AIN	TS27L4AIN
TLC27L4BCD	TS27L4BCD
TLC27L4BCN	TS27L4BCN
TLC27L4BID	TS27L4BID
TLC27L4BIN	TS27L4BIN
TLC27L4CD	TS27L4CD
TLC27L4CN	TS27L4CN
TLC27L4ID	TS27L4ID
TLC27L4IN	TS27L4IN
TLC27M2ACD	TS27M2ACD
TLC27M2ACP	TS27M2ACN
TLC27M2AID	TS27M2AID
TLC27M2AIP	TS27M2AIN
TLC27M2BCD	TS27M2BCD
TLC27M2BCP	TS27M2BCN
TLC27M2BID	TS27M2BID
TLC27M2BIP	TS27M2BIN
TLC27M2CD	TS27M2CD
TLC27M2CP	TS27M2CN
TLC27M2ID	TS27M21D
TLC27M2IP	TS27M2IN
TLC27M4ACD	TS27M4ACD
TLC27M4ACN	TS27M4ACN
TLC27M4AID	TS27M4AID
TLC27M4AIN	TS27M4AIN
TLC27M4BCD	TS27M4BCD
TLC27M4BCN	TS27M4BCN
TLC27M4BID	TS27M4BID
TLC27M4BIN	TS27M4BIN
TLC27M4CD	TS27M4CD
TLC27M4CN	TS27M4CN
TLC27M4ID	TS27M4ID
TLC27M4IN	TS27M4IN
TLC372CD	TS372CD
TLC372CP	TS372CN
TLC372ID	TS372ID
TLC372IP	TS372IN
TLC374CD	TS374CD
TLC374CN	TS374CN
TLC374ID	TS374ID
TLC374IN	TS374IN

THE RANGE

SUPPLY CURRENT OPTIONS

TS 271	PROGRAMMABLE	
TS 27x	HIGH	1mA
TS 27Mx	MEDIUM	150 µA
TS 27Lx	LOW	10 µA

2 PACKAGE TYPES

N	DIP	8, 14
D	SO	8, 14

3 OFFSET VOLTAGE SELECTIONS

TS 27x	10mV max.
TS 27xA	5mV max.
TS 27xB	2mV max.

3 CONFIGURATIONS

TS 271	SINGLE
TS 272	DUAL
TS 274	QUAD.

COMPARATORS

TS 372	DUAL.
TS 374	QUAD.

TIMERS*

3 TEMP. RANGES

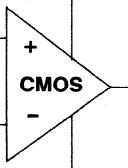
TS 27x C	0 to + 70°C
TS 27x I	-40 to + 105°C
TS 27x M	-55 to + 125°C

TO BE INTRODUCED 2H89

APPLICATIONS

SINGLE SUPPLY VOLTAGE
PORTABLE
SENSORS (PRESSURE, LEVEL, VOLUMETRIC)

LOW INPUT OFFSET VOLTAGE
COMPUTER



LOW SWITCH NOISE
TELECOM
INSTRUMENTATION

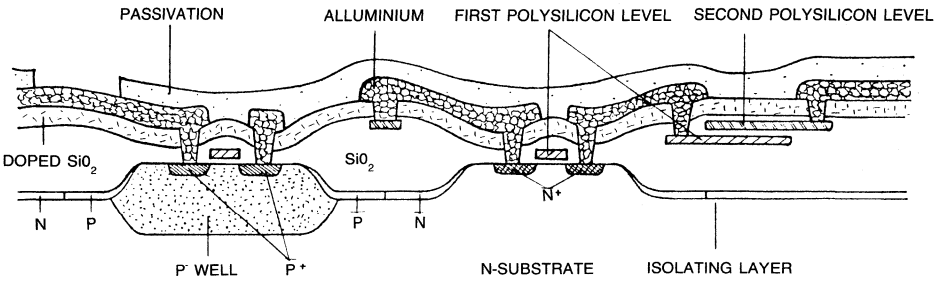
LOW INPUT CURRENT
INSTRUMENTATION
AUTO RADIO
TELECOM
SENSORS

LOW SUPPLY CURRENT
TELECOM
WHITE GOODS

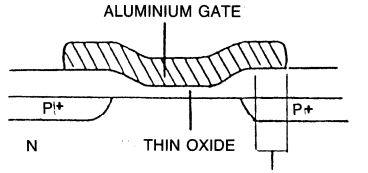
LOW SUPPLY VOLTAGE
TELECOM NETWORK

CMOS PROCESS

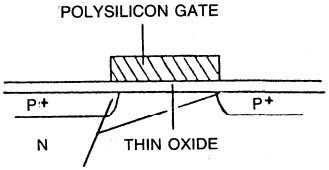
- 4 μm OR P - WELL WIDTH DUAL LAYER POLYSILICON GATE.
- PHOSPHORUS DOPED POLYSILICON GATES GIVE STABLE AND LOW INPUT OFFSET VOLTAGES BY TRAPPING FREE SODIUM IONS AT GATE/OXIDE OR OXIDE/SILICON INTERFACES.
- SELF ALIGNED GATES REDUCE GATE/DRAIN CAPACITANCE AND IMPROVE BANDWIDTH TO 2.5 MHz AND SLEW RATE TO 4.5 V/μS.
- ONLY 4 CRITICAL ALIGNMENTS ENSURE COST COMPETITIVENESS.



SELF ALIGNED GATE



DESIGNED OVERLAP TO AVOID MISALIGNMENT



NEGLIGIBLE OVERLAP

DRAIN/SOURCE DIFFUSION IS MADE BEFORE THE GATES ETCHING

DRAIN/SOURCE IS MADE AFTER THE GATES ETCHING, THE GATES HAVING A MASK FUNCTION DURING THE DIFFUSION. THE OVERLAP IS THEREFORE NEGLIGIBLE.

OPERATIONAL AMPLIFIERS

The CMOS Op.-Amps are low cost, low power operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.
Three power consumptions are available allowing to have always the best consumption-speed ratio.

- ICC = 10 μA per Amplifier: TS27LX (Low Supply Versions)
- ICC = 150 μA per Amplifier: TS27MX (Medium Supply Versions)
- ICC = 1 mA per Amplifier: TS27X (High Supply Versions)

The input impedance is similar to the J-FET input impedance: very high input impedance and extremely low input offset voltage and bias currents. They allow to minimize the static errors in low impedance applications.

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT FOR TS27X
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN COMPATIBLE TO STANDARD OPERATIONAL AMPLIFIERS
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (EDS) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS: STANDARD (10mV), A (5mV), B (2mV)

COMPARATORS

The CMOS comparators are low cost, low power comparator designed to operate with single or dual supplies. These comparators use the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption speed ratio. These series are ideally suited for low consumption applications.

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 4V to 10V or $\pm$ 2V to $\pm$5V.
- VERY LOW SUPPLY CURRENT: 0.4 mA INDEPENDENT OF SUPPLY VOLTAGE.
- EXTREMELY LOW INPUT OFFSET CURRENT: 1 pA TYP
- EXTREMELY LOW INPUT BIAS CURRENT: 1pA TYP.
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUPTUT SATURATION VOLTAGE 150 mV TYP
- OUTPUT COMPATIBLE WITH TTL MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE 10^{12} Ω TYP
- FAST REPONSE TIME: 200 ns TYP FOR TTL LEVEL INPUT STEP

SELECTION GUIDE

FEATURES	BENEFITS
■ VOLTAGE RANGE FROM 4V TO 10V (MAX = 12V)	■ ALLOWS DESIGN IN WIDE APPLICATION RANGE (FROM BATTERY OPERATION TYPE UP TO USUAL 12V SUPPLY VOLTAGE TYPE)
■ SINGLE SUPPLY VOLTAGE ■ ADAPTABLE BIAS CURRENT	■ AVOIDS NEGATIVE TYPE POWER SUPPLY ALLOWS BEST CONSUMPTION/SPEED RATIO (COST EFFECTIVENESS)
■ EXTREMELY LOW INPUT CURRENT (1pA)	■ MINIMIZES STATIC ERROR IN LOW IMPEDANCE APPLICATIONS
■ OFFSET VOLTAGE STABILITY (0.7 μV/C)	■ ANSWERS TO INSTRUMENTATION MARKET NEEDS WITH GENERAL PURPOSE TYPE PRICING.
■ ADAPTABLE BANDWIDTH AND SLEW RATE 0.04 | 0.6 | 5.5 | (V/μs) 0.1 | 1 | 3.5 | (MHz)	■ MORE PERFORMANCE REGARDING TO CONSUMPTION (0.35 MHz/mW) ALLOW SMALL SIZE POWER SUPPLY, LESS HEAT DISSIPATION, HIGHER RELIABILITY
■ DYNAMIC BEHAVIOUR - TS271/TS272/TS274 - TS271/TS27M2/TS27M4	■ EASY REPLACEMENT WITH BETTER BEHAVIOUR — OF JFET OP-AMPs FAMILY — OF BIPOLAR OP-AMPs FAMILY
■ SYMETRICAL OUTPUT CURRENT	■ ALLOWS USE OF IDENTICAL LOADS
■ LOW OUTPUT DYNAMIC IMPEDANCE	■ REDUCES SETTLING TIME
■ LINEARITY OF THE TRANSFER FUNCTION (IN SINGLE OR DUAL POWER SUPPLY UTILISATION)	■ LOWERS GAIN DISPERSION IN OPEN-LOOP OPERATION MODE
■ EXCELLENT PHASE MARGIN (DUE TO INTERNAL COMPENSATION)	■ IMPROVES THE STABILITY FOR HIGH CAPACITANCE LOAD (MORE THAN 100pF)
■ OFFSET NULL CAPABILITY (TS271)	■ MINIMIZES STATIC ERROR (WHEN USED IN COMPARATOR MODE)
■ LARGE AND CONTINUOUS PROGRAMMATION RANGE (FROM 1μA UP TO 200 μA) (TS271)	■ ALLOWS HIGH OPTIMISATION FOR ALL TYPES OF APPLICATIONS.

TS271 VERSUS COMPETITIVE OP-AMPs

Type	Technology	Main Feature	Single Supply	Operating Voltage (V)	Supply Current (mA) Max	Adjustable	Input Offset Voltage (mV) Max	Bandwidth (MHz) Typ	Slew Rate (V/µs) Typ
TS271	**C-MOS**	**Programmable**	**YES**	**+12**	**0.02-2**	**Offset**	**2-10**	**0.1-2.5**	**0.05-4.5**
TL061	JFET	Low Power	NO	±18	0.25	Offset	3-15	1	3.5
TL071	JFET	Low Noise	NO	±18	2.5	Offset	3-10	3	13
TL081	JFET	General Purpose	NO	±18	2.5	Offset	3-10	3	13
LF355	JFET	General Purpose	NO	±18	4	Offset	2	2.5	5
UA741	Bipolar	General Purpose	NO	±18	2.8	Offset	6	1	0.5
UA748	Bipolar	General Purpose	NO	±18	2.8	Offset Frequency	6		0.5
UA776	Bipolar	Programmable	NO	±18	0.02-0.19	Offset	6	0.01-1	0.03-0.8
LM301A	Bipolar	General Purpose	NO	±18	3	Offset Frequency	10		0.5
LM308A	Bipolar	Precision	NO	±18	0.8	Offset Frequency	0.5		0.5
LM318	Bipolar	Ultra Fast	NO	±20	10	Offset	10	15	70
TDB7910	Bipolar	Power	YES	±18	20	Offset Frequency	6	1	0.3

TS272 VERSUS COMPETITIVE OP-AMPs

Type	Technology	Main Feature	Single Supply	Operating Voltage (V)	Supply Current (mA) Max (Per amplifier)	Input Offset Voltage (mV) Max	Bandwidth (MHz) Typ	Slew Rate (V/µs) Typ
TS272	**C-MOS**	**Low Power**	**YES**	**+12**	**0.015-1.5**	**2-10**	**0.1-3.5**	**0.04-5.5**
TL062	JFET	Low Power	NO	±18	0.25	3-15	1	3.5
TL072	JFET	Low Noise	NO	±18	2.5	3-10	3	13
TL082	JFET	General Purpose	NO	±18	2.5	3-10	3	13
LM358	Bipolar	Low Power	YES	±16 or 32	1	3-7	1	0.6
LM2904	Bipolar	Low Power	YES	±13 or 26	1	7	1	0.6
LM1458	Bipolar	General Purpose	NO	±18	2.5	5	1	0.8
MC4558	Bipolar	Wide Band	NO	±18	2.5	6	2.8	1.6
TEB1033	Bipolar	High Stability	NO	±18	0.75	1	2.5	1

TS274 VERSUS COMPETITIVE OP-AMPs

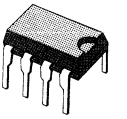
Type	Technology	Main Feature	Single Supply	Operating Voltage (V)	Supply Current (mA) Max (Per amplifier)	Input Offset Voltage (mV) Max	Bandwidth (MHz) Typ	Slew Rate (V/µs) Typ
TS274	**C-MOS**	**Low Power**	**YES**	**+12**	**0.015-1.5**	**2-10**	**0.1-3.5**	**0.04-5.5**
TL064	JFET	Low Power	NO	±18	0.25	3-15	1	3.5
TL074	JFET	Low Noise	NO	±18	2.5	3-10	3	13
TL084	JFET	General Purpose	NO	±18	2.5	3-10	3	13
LM324	Bipolar	Low Power	YES	±16 or 32	0.75	3-7	1	0.5
LM2902	Bipolar	Low Power	YES	±13 or 26	0.75	7	1	0.5
LM346	Bipolar	Programmable	NO	±18	0.625	6	1.2	0.4
LM348	Bipolar	Differential Input	NO	±18	0.9	5	1	0.5
MC3403	Bipolar	Differential Input	YES	±18 or 36	1	5	1	0.6
TEB4033	Bipolar	High Stability	NO	±18	0.75	1	2.5	1

DATASHEETS/RELIABILITY REPORT

OP-AMPs

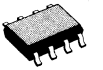
CMOS SINGLE OPERATIONAL AMPLIFIERS

- OFFSET NULL CAPABILITY (by external compensation)
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT
- THE TRANSFER FUNCTION IS LINEAR
- CONSUMPTION CURRENT AND DYNAMIC PARAMETERS ARE STABLE REGARDING THE VOLTAGE POWER SUPPLY VARIATIONS
- DYNAMIC CHARACTERISTICS ADJUSTABLE BY I_{set}
- VERY LARGE I_{set} RANGE
- PIN COMPATIBLE TO SINGLE OPERATIONAL AMPLIFIER (UA776)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



N
DIP8
(Plastic Package)

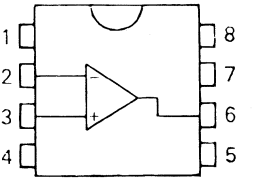
J
CERDIP8
(Cerdip Package)



D
SO8
(Plastic Micropackage)

(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS271-01

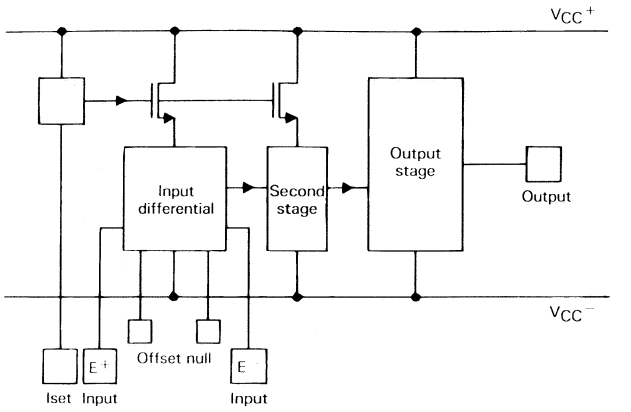
1 – Offset null 1
2 – Inverting input
3 – Non-inverting input
4 – V_{CC}^-
5 – Offset null 2
6 – Output
7 – V_{CC}^+
8 – I_{set}

DESCRIPTION

The TS271 is a low cost, low power single operational amplifier designed to operate with single or dual supplies. This operational amplifier uses the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving it an excellent consumption-speed ratio. This amplifier is ideally suited for low consumption applications.
The power supply is externally programmable with a resistor connected between pins 8 and 4. It allows to choose the best consumption-speed ratio and the consumption can be minimized according to the needed speed. These devices are specified for the following I_{set} current values : 1.5 µA, 25 µA, 130 µA.

The input impedance is similar to the J-FET input impedance : very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

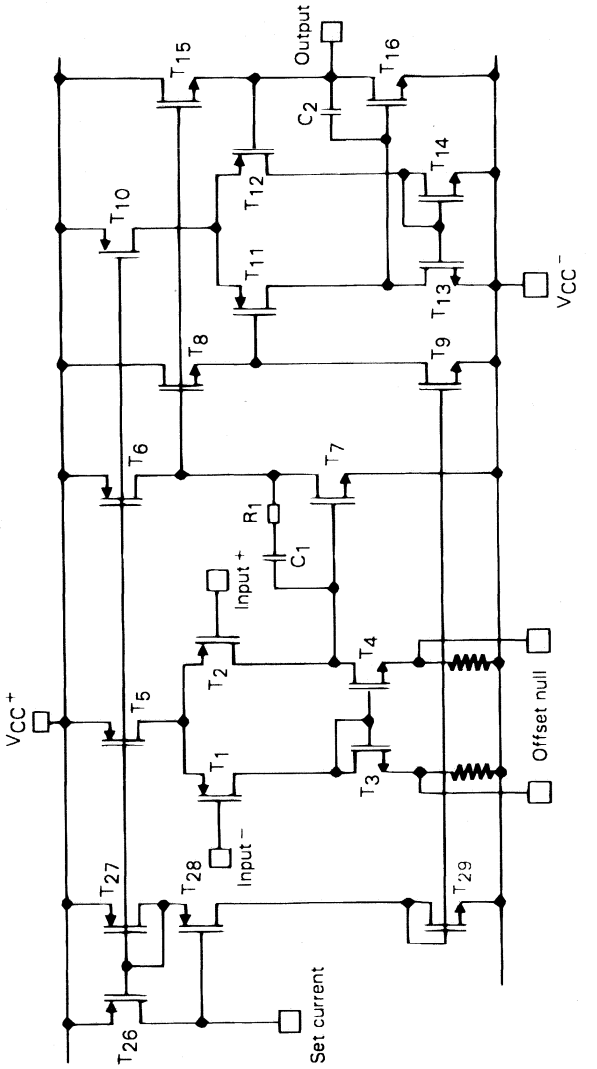
Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	12	V
V_{id}	Differential Input Voltage (note 2)	± 12	V
V_i	Input Voltage (note 3)	- 0.3 to 12	V
T_{oper}	Operating Free-air Temperature TS271C TS271I TS271M	0 to 70 - 40 to 105 - 55 to 125	°C
T_{stg}	Storage Temperature	- 65 to 150	°C
I_{set}	I_{set} Range	1 to 200	µA

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

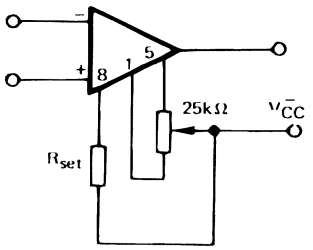
OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common-mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM



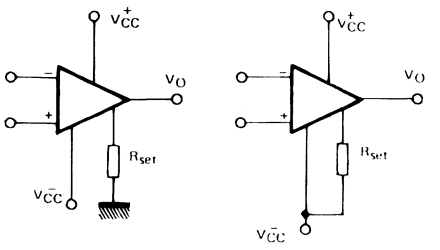
OFFSET VOLTAGE NULL CIRCUIT



E88TS271-04

OFFSET COMPENSATION GUARANTEED FOR TS271BCX (I_{set} > 25 µA), TS271ACX (I_{set} > 90 µA)

RESISTOR BIASING

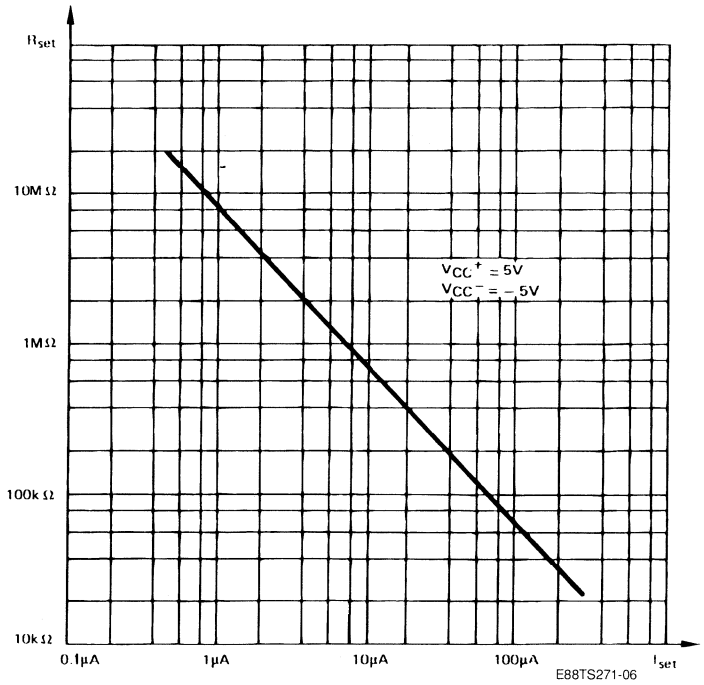


E88TS271-05

R_{set} CONNECTED TO GROUND

R_{set} CONNECTED TO V_{CC}^- (R_{set} VALUE : SEE FIG. 1)

Figure 1 : R_{set} Connected to V_{CC}^-.



E88TS271-06

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 1.5 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 mΩ $T_{min} < T < T_{max}$	8.8 8.7	9		8.8 8.6	9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 1 mΩ $T_{min} < T < T_{max}$	30 20	100		30 20	100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF fin = 10 KHz		0.1			0.1		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V, V_i = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 10 pF C_L = 100 pF		 35 10			 35 10		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 40 70			 40 70		%
V_n	Input Equivalent Noise Voltage F = 1 KHz R_S = 10 Ω		70			70		nV/√Hz

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 25 µA (unless otherwise specified)
R_L Connected to V_{CC}^-

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100KΩ $T_{min} < T < T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 100 KΩ $T_{min} < T < T_{max}$	30 20	50		30 10	50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 KΩ C_L = 100 pF fin = 100 KHz		0.7			0.7		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V , V_i = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 KΩ C_L = 10 pF C_L = 100 pF		 50 30			 50 30		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		 30 50			 30 50		%
V_n	Input Equivalent Noise Voltage F = 1 KHz R_S =10 Ω		38			38		nV/√Hz

Note : 1. Low output voltage is less than 50mV.

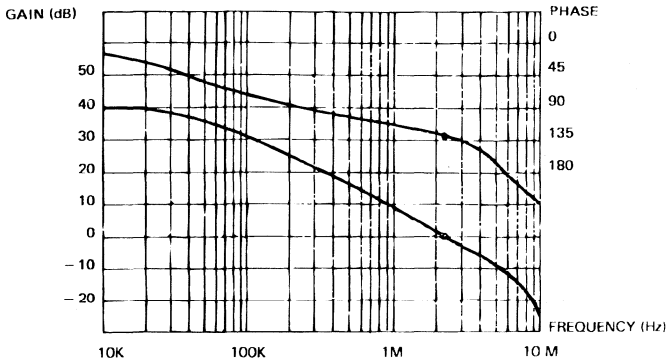
ELECTRICAL CHARACTERISTICS

T_{amb} = 25 °C, V_{CC} = 10 V, I_{set} = 130 µA (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS271C			TS271I, TS271M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS271 $T_{min} < T < T_{max}$ TS271A $T_{min} < T < T_{max}$ TS271B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 100		1	 200	pA
I_b	Input Bias Current V_i = 5 V , V_o = 5 V $T_{min} < T < T_{max}$		1	 150		1	 300	pA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 KΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 10 KΩ $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 KΩ C_L = 100 pF fin = 200 KHz		2.3			2.3		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	60	80		60	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V , V_i = 5 V $T_{min} < T < T_{max}$		800	1300 1400		800	1300 1500	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		4.5			4.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 KΩ C_L = 10 pF C_L = 100 pF		 56 56			 56 56		Degrees
K_{OV}	Overshoot Factor C_L = 10 pF C_L = 100 pF		30 30			30 30		%
V_n	Input Equivalent Noise Voltage F =1 KHz R_S = 10 Ω		30			30		nV/√Hz

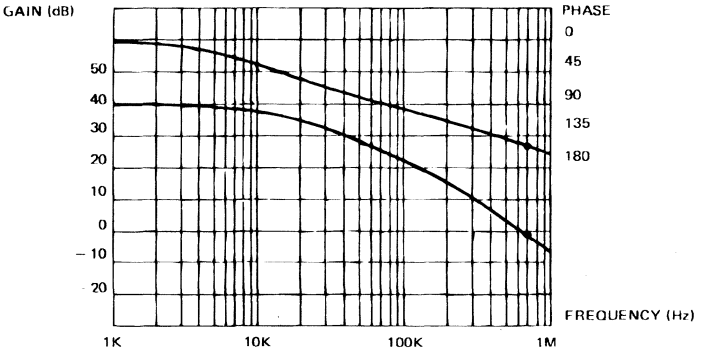
Note : 1. Low output voltage is less than 50mV.

I_{set} = 130 µA



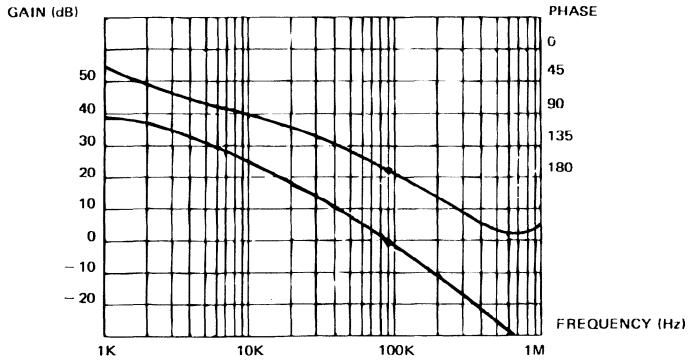
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
$V_{CC} \pm 5$ V, $R_L = 10$ KΩ, $C_L = 100$ pF, $T_{amb} = 25$ °C E88TS271-07

I_{set} = 25 µA



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
$V_{CC} \pm 5$ V, $R_L = 100$ KΩ, $C_L = 100$ pF, $T_{amb} = 25$ °C E88TS271-08

I_{set} = 1.5 µA



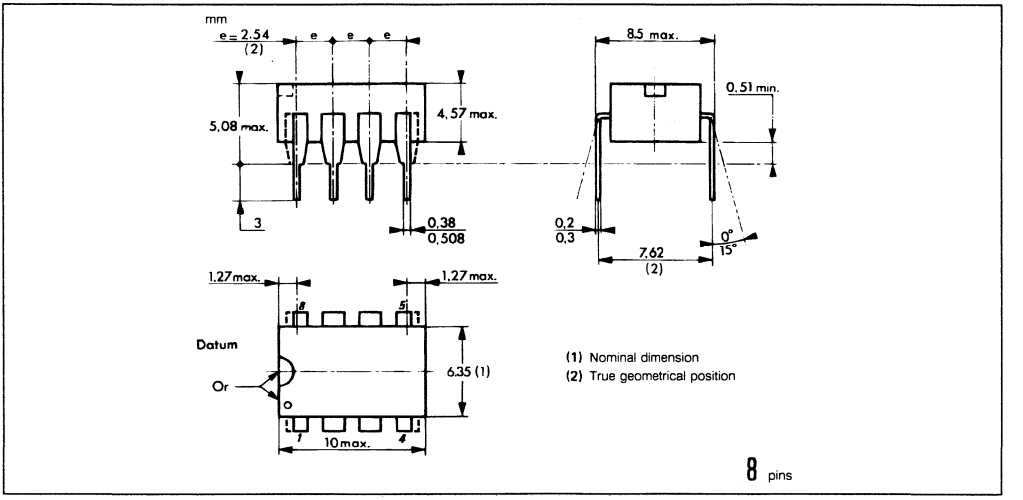
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
$V_{CC} \pm 5$ V, $R_L = 1$ MΩ, $C_L = 100$ pF, $T_{amb} = 25$°C E88TS271-09

ORDER CODES

Part Number	Temperature Range °C	Package		
		N	D	J
TS271C	0 to + 70	•	•	
TS271AC	0 to + 70	•	•	
TS271BC	0 to + 70	•	•	
TS271I	- 40 to + 105	•	•	
TS271M	- 55 to + 125			•
TS271AI	- 40 to + 105	•	•	
TS271AM	- 55 to + 125			•
TS271BI	- 40 to + 105	•	•	
TS271BM	- 55 to + 125			•
Examples : TS271 ACN, TS271 CD				

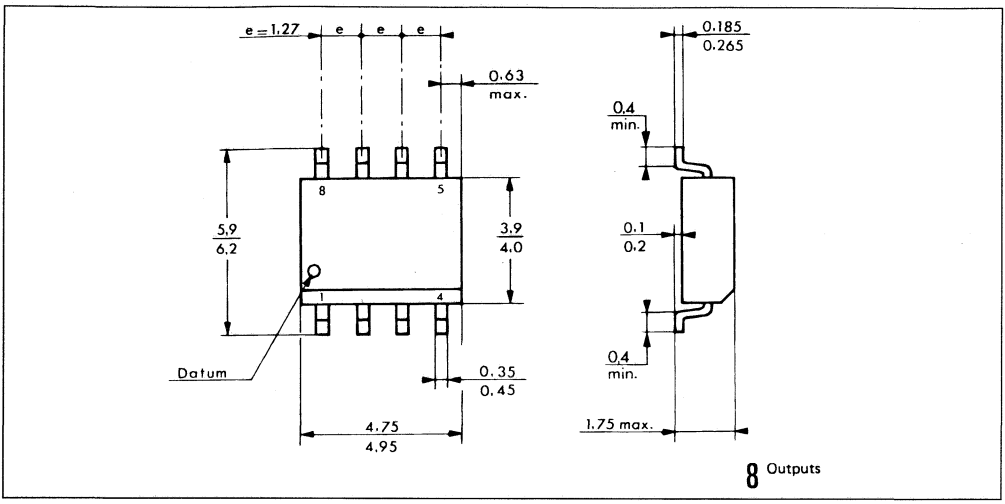
PACKAGE MECHANICAL DATA

8 PINS – PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

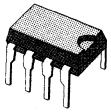
8 PINS – PLASTIC MICROPACKAGE SO



TS272
TS27M2/TS27L2

CMOS DUAL OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITANCE LOADS
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT FOR TS272
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN COMPATIBLE TO STANDARD DUAL OPERATIONAL AMPLIFIERS (TL082 - LM358)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



N
DIP8
(Plastic package)

J
CERDIP8
(Cerdip package)

D
SO8
(Plastic micropackage)

(Order Codes at the end of the Data sheet)

DESCRIPTION

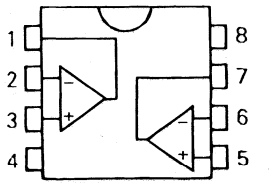
The TS272 series are low cost, low power dual operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio.

- I_{CC} = **10 µA** per amplifier : TS27L2 (Low bias versions)
- I_{CC} = **150 µA** per amplifier : TS27M2 (Medium bias versions)
- I_{CC} = **1 mA** per amplifier : TS272 (High bias versions)

The input impedance is similar to the J-FET input impedance. Very high input impedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

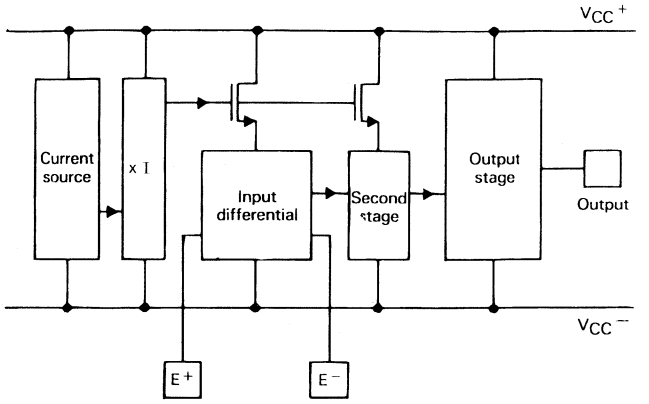
PIN CONNECTIONS (top view)



E88TS272-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

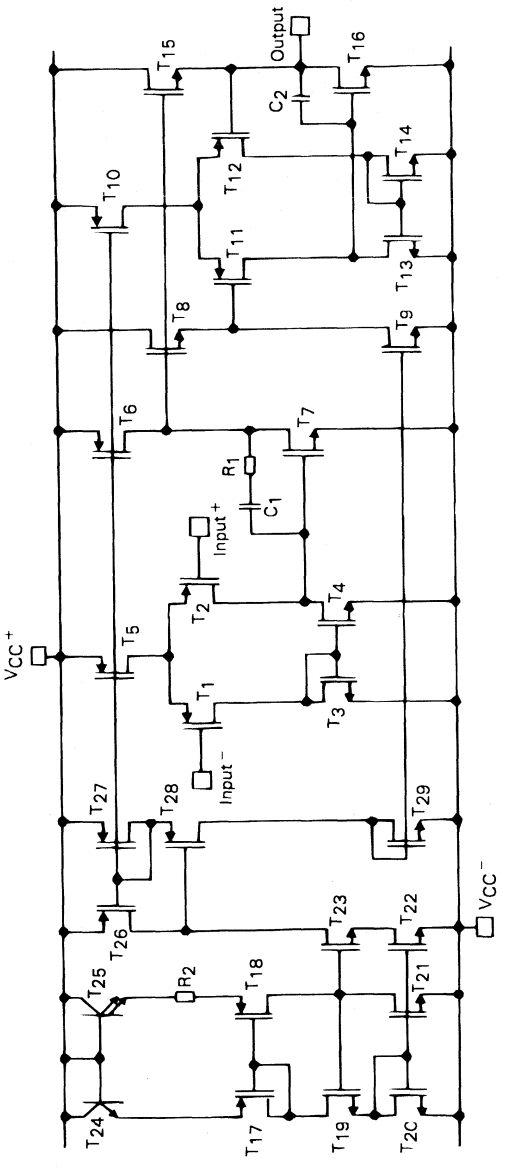
Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		− 0.3 to 12	V
T_{oper}	Operating Free-air Temperature			
		TS272C	0 to 70	°C
		TS272I	− 40 to 105	
		TS272M	− 55 to 125	
		TS27M2C	0 to 70	
		TS27M2I	− 40 to 105	
		TS27M2M	− 55 to 125	
		TS27L2C	0 to 70	
		TS27L2I	− 40 to 105	
		TS27L2M	− 55 to 125	
T_{stg}	Storage Temperature		− 65 to 150	°C

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal respect to the terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common Mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM (For 1/2 TS27×2)



E88TS272-03

ELECTRICAL CHARACTERISTICS FOR TS272

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} –

Symbol	Parameter	TS272C			TS272I/TS272M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS272 $T_{min} < T < T_{max}$ TS272A $T_{min} < T < T_{max}$ TS272B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 kΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V V_i = 5 V R_L = 10 KΩ $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 kΩ C_L = 100 pF Fin = 200 KHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_O = 5 V $T_{min} < T < T_{max}$		1000	1500 1600		1000	1500 1700	µA
I_s	Output Current V_i = 10 mV, V_O = 0 V	45	60	85	45	60	85	mA
I_s (sink)	Output Current V_i = – 10 mV, V_O = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		5.5			5.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		30			30		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27M2

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} −

Symbol	Parameter	TS27M2C			TS27M2I/TS27M2M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27M2 $T_{min} < T < T_{max}$ TS27M2A $T_{min} < T < T_{max}$ TS27M2B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100 kΩ $T_{min} < T < T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	30 20	50		30 10	50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 kΩ C_L = 100 pF Fin = 100 KHz		1			1		MHz
CMR	Common-mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{vo}	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		38			38		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

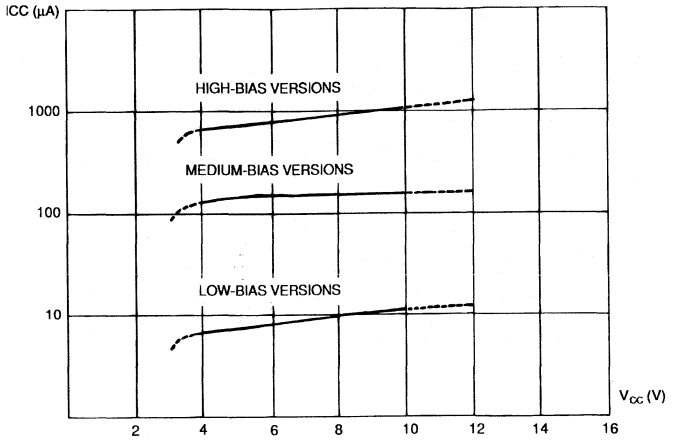
Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27L2

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} −

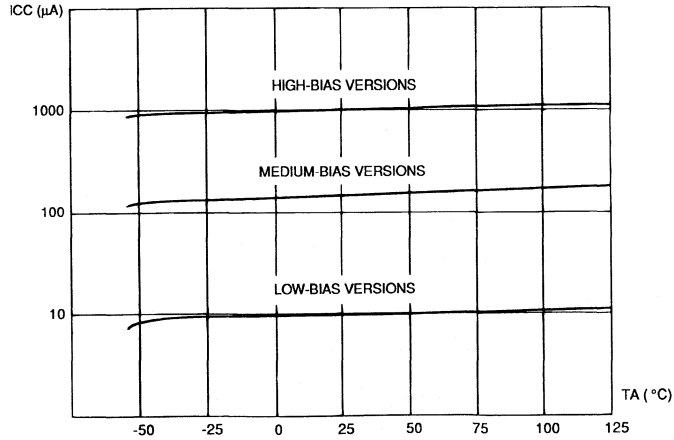
Symbol	Parameter	TS27L2C			TS27L2I/TS27L2M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27L2 $T_{min} < T < T_{max}$ TS27L2A $T_{min} < T < T_{max}$ TS27L2B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_{IB}	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 MΩ $T_{min} < T < T_{max}$	 8.8 8.7	 9		 8.8 8.6	 9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 1 MΩ V_i = 5 V $T_{min} < T < T_{max}$	 60 45	 100		 60 40	 100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF Fin = 100 KHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		70			70		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_O = V_{IC} = 0.2\ V_{CC}$, $T_{amb} = 25$ °C, NO LOAD

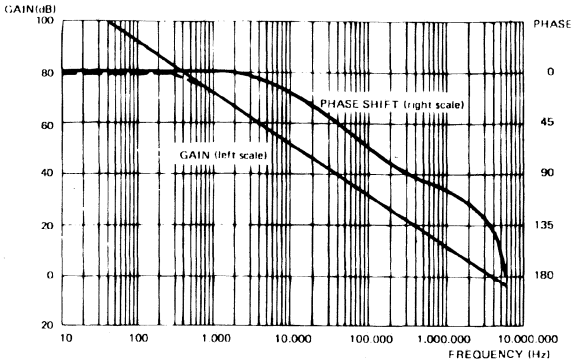
E88TS272-04



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_{CC} = 10$ V, $V_{IC} = 5$ V, $V_O = 5$ V, NO LOAD

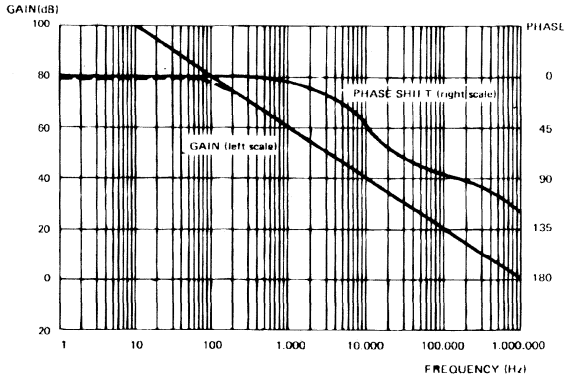
E88TS272-05

TS272



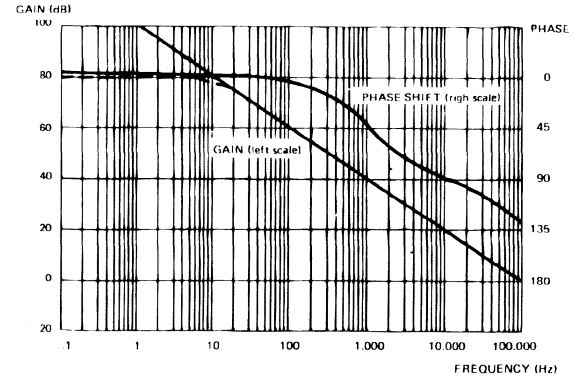
OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-06

TS27M2



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 100kΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-07

TS27L2



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 1MΩ, C_L = 100pF, T_{amb} = 25°C E88TS272-08

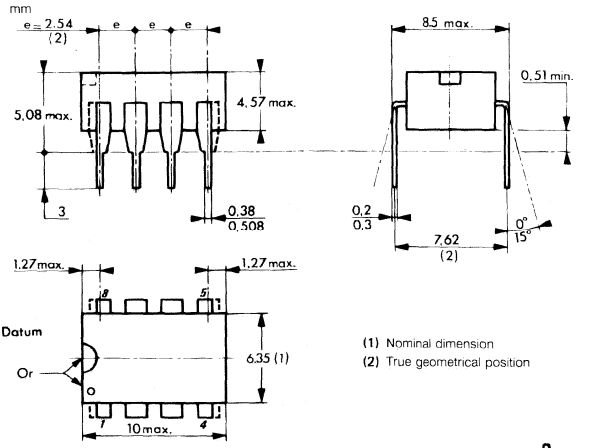
ORDER CODES

Part Number	Temperature Range °C	Package		
		N	D	J
TS272C	0 to 70	•	•	
TS272AC	0 to 70	•	•	
TS272BC	0 to 70	•	•	
TS272I	– 40 to 105	•	•	
TS272M	– 55 to 125			•
TS27M2C	0 to 70	•	•	
TS27M2AC	0 to 70	•	•	
TS27M2BC	0 to 70	•	•	
TS27M2I	– 40 to 105	•	•	
TS27M2M	– 55 to 125			•
TS27L2C	0 to 70	•	•	
TS27L2AC	0 to 70	•	•	
TS27L2BC	0 to 70	•	•	
TS27M2I	– 40 to 105	•	•	
TS27L2M	– 55 to 125			•
TS272AI	– 40 to 105	•	•	
TS272BI	– 40 to 105	•	•	
TS272AM	– 55 to 125			•
TS272BM	– 55 to 125			•
TS27M2AI	– 40 to 105	•	•	
TS27M2BI	– 40 to 105	•	•	
TS27L2AI	– 40 to 105	•	•	
TS27L2BI	– 40 to 105	•	•	
TS27M2AM	– 55 to 125			•
TS27M2BM	– 55 to 125			•
TS27L2AM	– 55 to 125			•
TS27L2BM	– 55 to 125			•

Examples : TS27L2ACN, TS272CD

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP

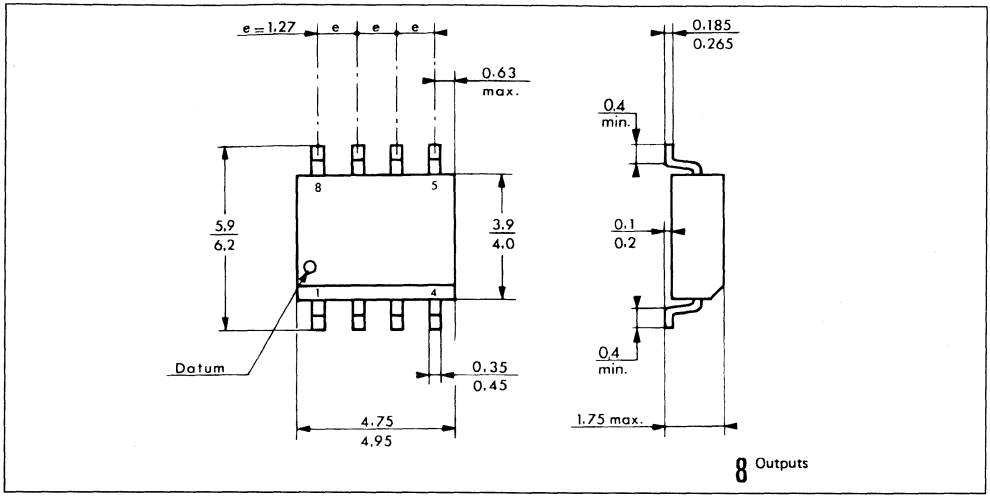


(1) Nominal dimension
(2) True geometrical position

8 pins

PACKAGE MECHANICAL DATA (continued)

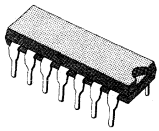
8 PINS - PLASTIC MICROPACKAGE SO



TS274
TS27M4/TS27L4

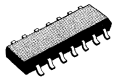
CMOS QUAD OPERATIONAL AMPLIFIERS

- EXCELLENT PHASE MARGIN ON CAPACITIVE LOADS
- SYMMETRICAL OUTPUT CURRENTS
- HIGH GAIN BANDWIDTH PRODUCT FOR TS274
- LOW OUTPUT DYNAMIC IMPEDANCE
- THE TRANSFER FUNCTION IS LINEAR
- PIN COMPATIBLE TO STANDARD QUAD OPERATIONAL AMPLIFIERS (TL084-LM324)
- STABLE AND LOW OFFSET VOLTAGE
- INTERNAL ELECTROSTATIC DISCHARGE (ESD) PROTECTION CIRCUITS
- THREE INPUT OFFSET VOLTAGE SELECTIONS : STANDARD (10 mV), A (5 mV), B (2 mV)



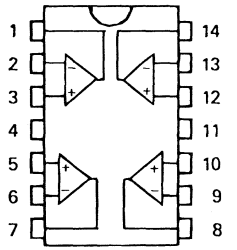
N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)
(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS274-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting input 1
4 - V_{CC}^+
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - Output 3
9 - Inverting input 3
10 - Non-inverting input 3
11 - V_{CC}^-
12 - Non-inverting input 4
13 - Inverting input 4
14 - Output 4

DESCRIPTION

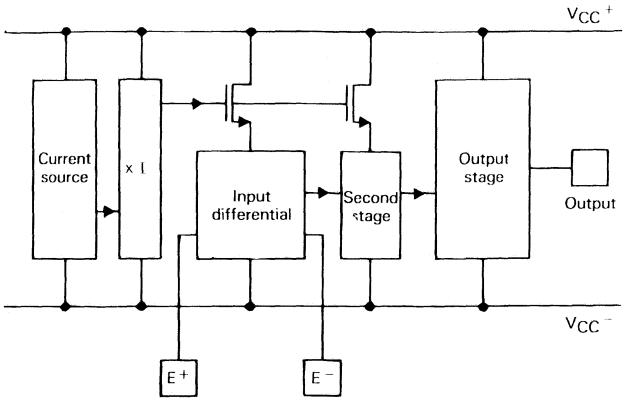
The TS274 series are low cost, low power quad operational amplifiers designed to operate with single or dual supplies. These operational amplifiers use the SGS-THOMSON Microelectronics silicon gate LIN MOS process giving them an excellent consumption-speed ratio. These series are ideally suited for low consumption applications.

Three power consumptions are available allowing to have always the best consumption-speed ratio.

- I_{CC} = **10 µA** per amplifier : TS27L4 (Low bias versions)
- I_{CC} = **150 µA** per amplifier : TS27M4 (Medium bias versions)
- I_{CC} = **1 mA** per amplifier : TS274 (High bias versions)

The input impedance is similar to the J-FET input impedance : very high input inpedance and extremely low input offset and bias currents. They allow to minimize the static errors in low impedance applications.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

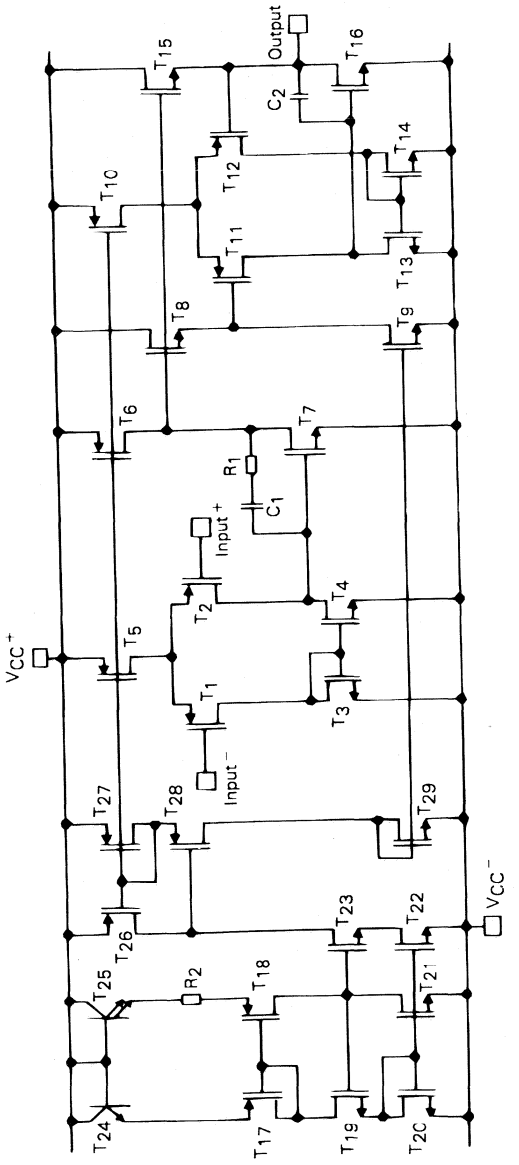
Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		- 0.3 to 12	V
T_{oper}	Operating Free-air Temperature			
		TS274C	0 to 70	°C
		TS274I	- 40 to 105	
		TS274M	- 55 to 125	
		TS27M4C	0 to 70	
		TS27M4I	- 40 to 105	
		TS27M4M	- 55 to 125	
		TS27L4C	0 to 70	
		TS27L4I	- 40 to 105	
		TS27L4M	- 55 to 125	
T_{stg}	Storage Temperature		- 65 to 150	°C

Notes : 1. All voltage values, except differential voltages, are with respect to network ground terminal.
2. Differential voltages are at the noninverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.

OPTIMAL OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage (note 1)	4 to 10	V
V_i	Common Mode Input Voltage V_{CC} = 10 V	0 to 9	V

SCHEMATIC DIAGRAM (for 1/4 TS27 x 4)



E88TS272-03

ELECTRICAL CHARACTERISTICS FOR TS274

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS274C			TS274I/TS274M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS274 $T_{min} < T < T_{max}$ TS274A $T_{min} < T < T_{max}$ TS274B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		5			5		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 10 kΩ $T_{min} < T < T_{max}$	8.2 8.1	8.4		8.2 8	8.4		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 10 kΩ V_i = 5 V $T_{min} < T < T_{max}$	10 7	15		10 6	15		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 10 kΩ C_L = 100 pF fin = 200 KHz		3.5			3.5		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	70		60	70		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		1000	1500 1600		1000	1500 1700	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		5.5			5.5		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 10 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		30			30		nV/√Hz
V_{O1}/V_{O2}	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27M4

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

Symbol	Parameter	TS27M4C			TS27M4I/TS27M4M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27M4 $T_{min} < T < T_{max}$ TS27M4A $T_{min} < T < T_{max}$ TS27M4B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		2			2		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 100 kΩ $T_{min} < T < T_{max}$	8.7 8.6	8.9		8.7 8.5	8.9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	30 20	50		30 10	50		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 100 kΩ C_L = 100 pF f_{in} = 100 KHz		1			1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		150	200 250		150	200 300	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
$S_{V\,O}$	Slew Rate at Unity Gain		0.6			0.6		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 100 kΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		38			38		nV/√Hz
V_{01}/V_{02}	Cross Talk Attenuation		120			120		dB

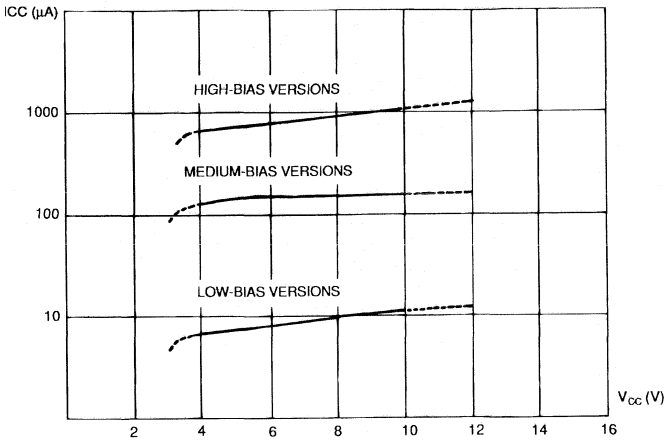
Note : 1. Low output voltage is less than 50mV.

ELECTRICAL CHARACTERISTICS FOR TS27L4

T_{amb} = 25 °C, V_{CC} = 10 V (unless otherwise specified)
R_L Connected to V_{CC} -

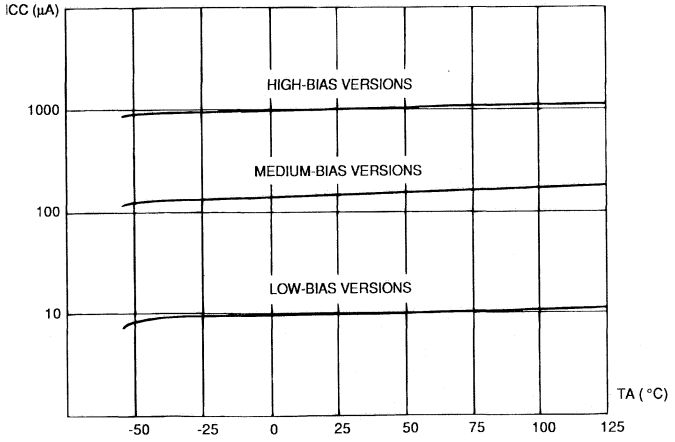
Symbol	Parameter	TS27L4C			TS27L4I/TS27L4M			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
V_{io}	Input Offset Voltage V_o = 1.4 V TS27L4 $T_{min} < T < T_{max}$ TS27L4A $T_{min} < T < T_{max}$ TS27L4B $T_{min} < T < T_{max}$			 10 12 5 6.5 2 3.5			 10 12 5 6.5 2 3.5	mV
αV_{io}	Temperature Coefficient of Input Voltage		0.7			0.7		µV/°C
I_{io}	Input Offset Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.1		1	 0.2	pA nA
I_b	Input Bias Current V_i = 5 V, V_o = 5 V $T_{min} < T < T_{max}$		1	 0.15		1	 0.3	pA nA
V_{DH}	High Output Voltage (note 1) V_i = 10 mV R_L = 1 MΩ $T_{min} < T < T_{max}$	8.8 8.7	9		8.8 8.6	9		V
A_{vd}	Large Signal Voltage Gain V_o = 1 V to 6 V R_L = 100 kΩ V_i = 5 V $T_{min} < T < T_{max}$	60 45	100		60 40	100		V/mV
G_{wr}	Gain Bandwidth Product A_v = 40 dB R_L = 1 MΩ C_L = 100 pF fin = 10 KHz		0.1			0.1		MHz
CMR	Common Mode Rejection Ratio V_o = 1.4 V V_i = 1 V to 7.4 V	65	80		65	80		dB
SVR	Supply Voltage Rejection Ratio V_{CC} = 5 V to 10 V V_o = 1.4 V	60	80		60	80		dB
I_{CC}	Supply Current (per amplifier) A_V = 1, no Load V_o = 5 V $T_{min} < T < T_{max}$		10	15 17		10	15 18	µA
I_s	Output Current V_i = 10 mV, V_o = 0 V	45	60	85	45	60	85	mA
I_s (Sink)	Output Current V_i = - 10 mV, V_o = V_{CC}	35	45	65	35	45	65	mA
S_{VO}	Slew Rate at Unity Gain		0.04			0.04		V/µS
ø m	Phase Margin at Unity Gain A_V = 40 dB R_L = 1 MΩ C_L = 100 pF		45			45		Degrees
K_{OV}	Overshoot Factor		30			30		%
V_n	Input Equivalent Noise Voltage f = 1 KHz R_S = 10 Ω		70			70		nV/√Hz
$\lvert V_{O1} / V_{O2} \rvert$	Cross Talk Attenuation		120			120		dB

Note : 1. Low output voltage is less than 50mV.



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_O = V_{IC} = 0.2\ V_{CC}$, $T_{amb} = 25$ °C, NO LOAD

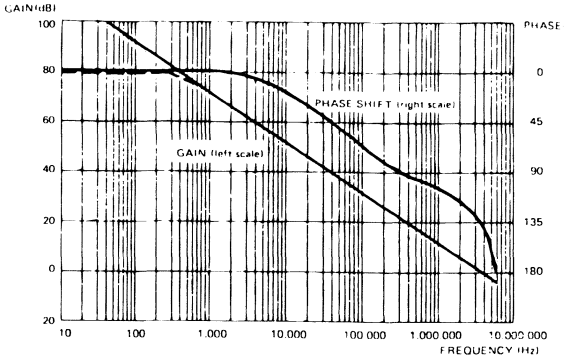
E88TS274-02



SUPPLY CURRENT vs FREE-AIR TEMPERATURE
$V_{CC} = 10$ V, $V_{IC} = 5$ V, $V_O = 5$ V, NO LOAD

E88TS274-03

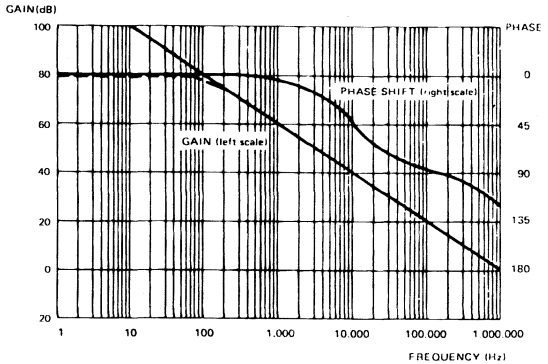
TS274



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 10kΩ, C_L = 100pF, T_{amb} = 25°C

E88TS274-04

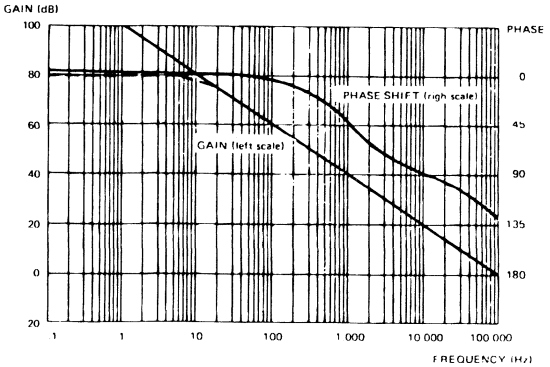
TS27M4



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 100kΩ, C_L = 100pF, T_{amb} = 25 °C

E88TS274-05

TS27L4



OPEN LOOP FREQUENCY RESPONSE AND PHASE SHIFT
V_{CC} = 10V, R_L = 1MΩ, C_L = 100pF, T_{amb} = 25°C

E88TS274-06

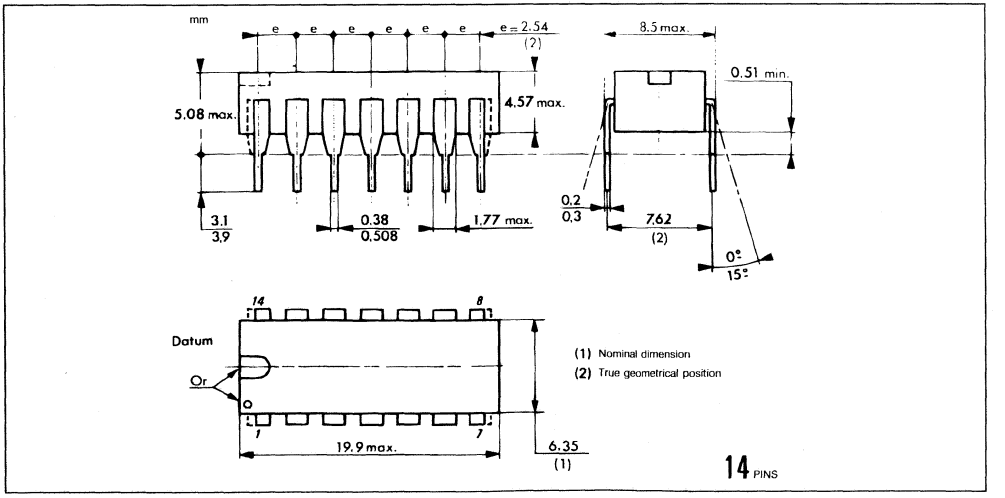
ORDER CODES

Part Number	Temperature Range °C	Package		
		N	D	J
TS274C	0 to + 70	•	•	
TS274AC	0 to + 70	•	•	
TS274BC	0 to + 70	•	•	
TS274I	- 40 to + 105	•	•	
TS274M	- 55 to + 125			•
TS27M4C	0 to + 70	•	•	
TS27M4AC	0 to + 70	•	•	
TS27M4BC	0 to + 70	•	•	
TS27M4I	- 40 to + 105	•	•	
TS27M4M	- 55 to + 125			•
TS27L4C	0 to + 70	•	•	
TS27L4AC	0 to + 70	•	•	
TS27L4BC	0 to + 70	•	•	
TS27M4I	- 40 to + 105	•	•	
TS27L4M	- 55 to + 125			•
TS27M4AI	- 40 to + 105	•	•	
TS27M4AM	- 55 to + 125			•
TS27M4BI	- 40 to + 105	•	•	
TS27M4BM	- 55 to + 125			•
TS27L4AI	- 40 to + 105	•	•	
TS27L4AM	- 55 to + 125			•
TS27L4BI	- 40 to + 105	•	•	
TS27L4BM	- 55 to ± 125			•

Examples : TS27L4ACN, TS274CD

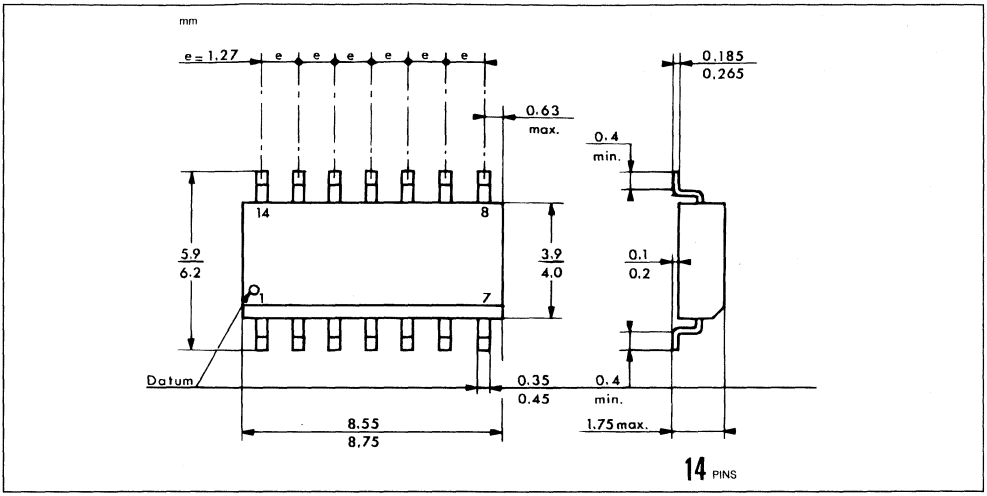
PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



PACKAGE MECHANICAL DATA (continued)

14 PINS - PLASTIC MICROPACKAGE SO



RELIABILITY REPORT

TECHNOLOGICAL CHARACTERISTICS

DIE:

- TECHNOLOGY: Silicon Gate LIN MOS Process
- METALIZATION: Al Si
- PASSIVATION: Doped Oxide

PACKAGE:

- DIE ATTACH: Glue
- LEAD FRAME MATERIAL: Copper
- LEAD COATING: Sn/Pb
- BOND PROCESS: Ball Bonding
- BOND MATERIAL: Au
- DIAMETER: 25 μm
- MOULDING PROCESS: Transfer
- MOULDING MATERIAL: Epoxy Resin NITTO HC10-2

TEST DESCRIPTION

A - Electrical Tests (Die Oriented Tests)

STATIC LIFE TEST: This test was performed to point out die problems connected to the surface contamination and to the layout structure.
The test conditions were:

V_S = 10V T_A = 125DG
T_J = 135DG

The devices were assembled in DIL plastic package or SO package.

B - Environment Tests (Package Oriented Tests)

To evaluate the moisture resistance and thermo-mechanical behaviour, we have performed a reliability characterization including the following tests:

- Temperature Humidity Bias (T.H.B.)
- Pressure Cooker Test (pressure pot)
- Temperature Cycling -55/150DG

ELECTRICAL RELIABILITY TESTS RESULTS

(Period: Year 87/1st half 88)

Test Conditions	Time	Sample Size	Rejects
LIFE TEST:			
* V_{CC} = +10V	1000H	440	0
* T_A = 125°C	2000H	360	0

V_{IN} = +10V for 50% of the devices
V_{IN} = 0V for 50% of the devices
(See fig. 1)

ENVIRONMENTAL RELIABILITY TESTS RESULTS

(Period: Year 87/1st half 88)

TEMPERATURE HUMIDITY BIAS

Test Conditions	Time	Sample Size	Rejects
DIP PACKAGE * V_{CC} = +10V * 85°C 85% R.H.	1000H	140	0
SO PACKAGE * V_{CC} = +10V * 85°C 85% R.H.	1000H	180	0

V_{IN} = +10V for 50% of the devices
V_{IN} = 0V for 50% of the devices.

PRESSURE POT

Test Conditions	Sample Size	Rejects	Package
T_A = 121°C P = 2.08ATM T = 168H	400	0	DIP
	480	0	SO

TEMPERATURE CYCLING

Test Conditions	Sample Size	Rejects	Package
400 cycles (T_A = —55°C to +150°C) 10 min. at extreme temperature, 5 min. max. transfer time.	200	0	DIP
	350	0	SO

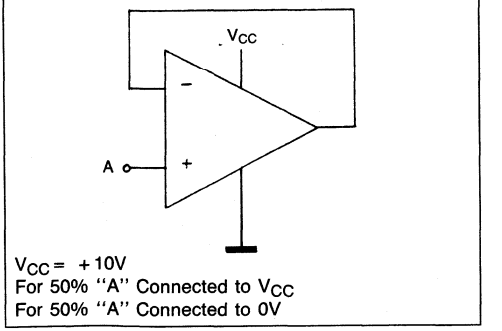
FAILURE RATE CALCULATION AT:

- T_J max (observed value and at 60% CL)
- T_J 55°C (at 60% CL)

At T_J = 135°C $\lambda = 1.14 \times 10^{-6} \cdot H^{-1}$
At T_J = 55°C λ = 1.2 Fits (Ea = 1 eV)

CIRCUIT CONFIGURATION

Figure 1 - THB Bias Life Test



V_{CC} = +10V
For 50% "A" Connected to V_{CC}
For 50% "A" Connected to 0V

FAILURE RATE CALCULATION

Reliability evaluation of a device means also failure rate (λ) evaluation, both during infant mortality and useful life.

The typical reliability test used for failure rate evaluation is H.T.R.B.

In its simple form the failure rate is:

$$\lambda = \frac{C}{N \cdot T} \quad (1)$$

Where λ = Failure rate (at a given temperature)
C = Number of failures
N = Number of tested devices
T = Number of test hours

When a low number of samples has been employed (as during homologation tests) and when a proper confidence level is required in order to estimate a correct λ value we suggest accepting a value C' obtained by Table 1 instead of C = number of failure employed in previous formula (1).
The new value for λ will be:

$$\lambda = \frac{C' \text{ (EXTRACTED BY TABLE 1)}}{N \cdot T}$$

Table 1

Number of Failure	CONFIDENCE LEVEL					
	50%	60%	70%	80%	90%	95%
0	0.693	0.916	1.204	1.660	2.305	2.990
1	1.678	2.022	2.439	2.990	3.890	4.740
2	2.674	3.120	3.615	4.280	5.300	6.300
3	3.672	4.160	4.762	5.500	6.700	7.750
4	4.671	5.250	5.891	6.700	8.000	9.150
5	5.670	6.300	7.005	7.900	9.250	10.50
6	6.669	7.350	8.111	9.100	10.55	11.85
7	7.669	8.400	9.209	10.25	11.75	13.15
8	8.669	9.450	10.30	11.40	13.00	14.45
9	9.668	10.50	11.38	12.50	14.20	15.70
10	10.66	11.55	12.47	13.65	15.40	16.95

To determine failure rate at other temperatures an acceleration factor F must be used.

F is determined, for a given thermal activation energy Ea, by the Arrhenius relationship as:

$$F(T_1, T_2) = \text{EXP}\left[-\frac{Ea}{K}\left(\frac{1}{T_1} - \frac{2}{T_2}\right)\right]$$

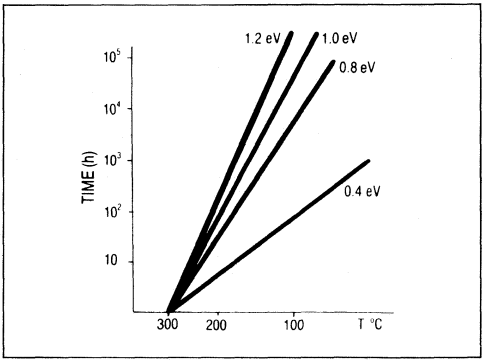
Where Ea = Thermal activation energy (eV)
K = Boltzmann's constant (8.63×10^{-5} eV/K)
T = Absolute temperature in °K

$$\lambda = (T_1) = F(T_1, T_2) \cdot \lambda (T_2)$$

Where $T_1 < T_2$

Fig. 2 shows temperature derating curves and multiplying factors for temperature reduction. The various lines correspond to the activation energies associated with the different failure mechanisms involved.

Figure 2 - Arrhenius Plot



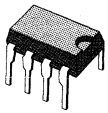
DATASHEETS

COMPARATORS

CMOS DUAL DIFFERENTIAL COMPARATOR

ADVANCED DATA

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 4V TO 10V OR ± 2V TO ± 5V
- VERY LOW SUPPLY CURRENT : 0.4 mA INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT : 1 pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1 pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150 mV TYP
- OUTPUT COMPATIBLE WITH TTL.MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE 10^{12} ΩTYP
- FAST REPONSE TIME : 200 NS TYP FOR TTL LEVEL INPUT STEP



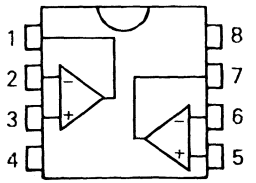
N
DIP14
(Plastic Package)

J
CERDIP14
(Cerdip Package)

D
SO14
(Plastic Micropackage)

(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



E88TS272-01

1 - Output 1
2 - Inverting input 1
3 - Non-inverting Input 1
4 - V_{CC}^-
5 - Non-inverting input 2
6 - Inverting input 2
7 - Output 2
8 - V_{CC}^+

DESCRIPTION

These devices consist of two independent precision voltage comparators, designed to operate with single or dual supplies.

These differential comparators use the SGS THOMSON Microelectronics silicon lin MOS process giving them an excellent consumption-speed ratio.

These devices are ideally suited for low consumption applications.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		12	V
V_O	Output Voltage		12	V
I_O	Output Current		20	mA
	Duration of Output Short-circuit to GND (note 4)		Unlimited	
T_{oper}	Operating Free-air Temperature	TS372C TS372I TS372M	0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature		– 65 to 150	°C

Notes : 1. All voltage values, except differential voltages are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	4 to 10	V
V_{CC}	Min Supply Voltage (for selected devices)	3	V
V_{CC}	Max Supply Voltage	12	V

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5 V, T = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage for $V_{IC} = V_{ICR\ Min}$ (note 1)		2	10	mV
I_{io}	Input Offset Current (note 1)		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Mode Voltage Range	0 to V_{CC} – 1.5 V			V
A_{vd}	Large Signal Voltage Gain V_{CC} = 10 V ; R_L > 15 KΩ at V_{CC}		200		V/mV
I_{oh}	High Level Output Current V_{id} = 1 V ; V_{oh} = + 5 V		0.1		nA
V_{ol}	Low Level Output Voltage V_{id} = 1 V ; I_{ol} = 4 mA		150	400	mV
I_{CC}	Supply Current (4 comparators) V_{id} = – 1 V ; R_L = ∞		0.4	1	mA
I_{ol}	Low Level Output Current V_{id} = – 1 V ; V_{OL} = 1.5 V	6	16		mA
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF Overdrive 5 mV (note 2)		600		ns
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF TTL Input (note 2)		200		ns

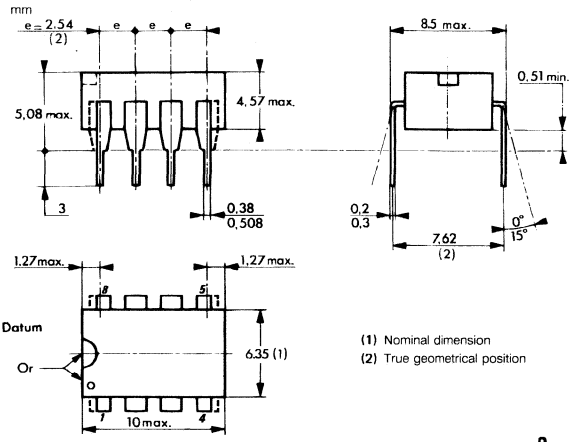
Notes : 1. The offset voltage and offset current which are given are the maximum values required to drive the output down to 400 mV or up to 4 V with R_L = 2.5 KΩ to V_{CC}.
2. The response time which is specified is the interval between the input signal and the instant when the output signal crosses 1.4 V.

ORDER CODES

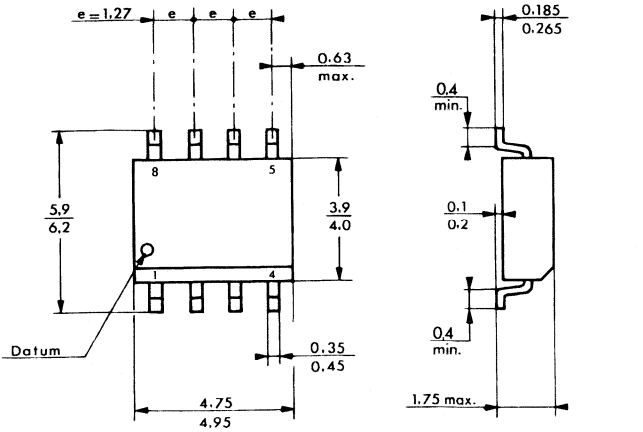
Part Number	Temperature Range	Package		
		N	D	J
TS372	0 to 70	•	•	
TS372I	– 40 to 105	•	•	
TS372M	– 55 to 125			•
Examples : TS372ID				

PACKAGE MECHANICAL DATA

8 PINS - PLASTIC DIP OR CERDIP



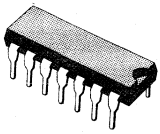
8 PINS - PLASTIC MICROPACKAGE SO



CMOS QUAD DIFFERENTIAL COMPARATOR

ADVANCED DATA

- WIDE SINGLE SUPPLY RANGE OR DUAL SUPPLIES 4V TO 10V OR ± 2V TO ± 5V
- VERY LOW SUPPLY CURRENT : 0.4 mA INDEPENDENT OF SUPPLY VOLTAGE
- EXTREMELY LOW INPUT BIAS CURRENT : 1 pA TYP
- EXTREMELY LOW INPUT OFFSET CURRENT : 1 pA TYP
- LOW INPUT OFFSET VOLTAGE
- INPUT COMMON-MODE VOLTAGE RANGE INCLUDES GND
- LOW OUTPUT SATURATION VOLTAGE 150 mV TYP
- OUTPUT COMPATIBLE WITH TTL.MOS AND CMOS
- BUILT-IN ESD PROTECTION
- HIGH INPUT IMPEDANCE 10^{12} ΩTYP
- FAST REPONSE TIME : 200 NS TYP FOR TTL LEVEL INPUT STEP



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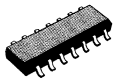
(Plastic Package)

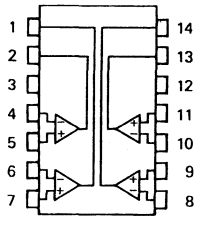
J
CERDIP14
(Cerdip Package)



D
SO14
(Plastic Micropackage)

(Order Codes at the end of the datasheet)

PIN CONNECTIONS (top view)



E88J374-01

1 - Output 2
2 - Output 1
3 - V_{CC}^+
4 - Inverting input 1
5 - Non-inverting input 1
6 - Inverting input 2
7 - Non-inverting input 2
8 - Inverting input 3
9 - Non-inverting input 3
10 - Inverting input 4
11 - Non-inverting input 4
12 - V_{CC}^-
13 - Output 4
14 - Output 3

DESCRIPTION

These devices consist of four independent precision voltage comparators, designed to operate with single or dual supplies.

These differential comparators use the SGS THOMSON Microelectronics silicon lin MOS process giving them an excellent consumption-speed ratio.

These devices are ideally suited for low consumption applications.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	Supply Voltage (note 1)		12	V
V_{id}	Differential Input Voltage (note 2)		± 12	V
V_i	Input Voltage (note 3)		12	V
V_O	Output Voltage		12	V
I_O	Output Current		20	mA
	Duration of Output Short-circuit to GND (note 4)		Unlimited	
T_{oper}	Operating Free-air Temperature	TS374C TS374I TS374M	0 to 70 – 40 to 105 – 55 to 125	°C
T_{stg}	Storage Temperature		– 65 to 150	°C

Notes : 1. All voltage values, except differential voltages are with respect to network ground terminal.
2. Differential voltages are at the non-inverting input terminal with respect to the input terminal.
3. The magnitude of the input voltage must never exceed the magnitude of the positive supply voltage.
4. Short circuit from outputs to V_{CC}^+ can cause excessive heating and eventual destruction.

OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage Range	4 to 10	V
V_{CC}	Min Supply Voltage (for selected devices)	3	V
V_{CC}	Max Supply Voltage	12	V

ELECTRICAL CHARACTERISTICS (V_{CC} = + 5 V, T = 25 °C)

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
V_{io}	Input Offset Voltage for $V_{IC} = V_{ICR\ Min}$ (note 1)		2	10	mV
I_{io}	Input Offset Current (note 1)		1		pA
I_{ib}	Input Bias Current		1		pA
V_{ICR}	Input Common Mode Voltage Range	0 to V_{CC} – 1.5 V			V
A_{vd}	Large Signal Voltage Gain V_{CC} = 10 V ; R_L > 15 KΩ at V_{CC}		200		V/mV
I_{oh}	High Level Output Current V_{id} = 1 V ; V_{oh} = + 5 V		0.1		nA
V_{ol}	Low Level Output Voltage V_{id} = 1 V ; I_{ol} = 4 mA		150	400	mV
I_{CC}	Supply Current (4 comparators) V_{id} = – 1 V ; R_L = ∞		0.4	1	mA
I_{ol}	Low Level Output Current V_{id} = – 1 V ; V_{OL} = 1.5 V	6	16		mA
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF Overdrive 5 mV (note 2)		600		ns
T_{re}	Response Time R_L = 5.1 KΩ ; C_L = 15 pF TTL Input (note 2)		200		ns

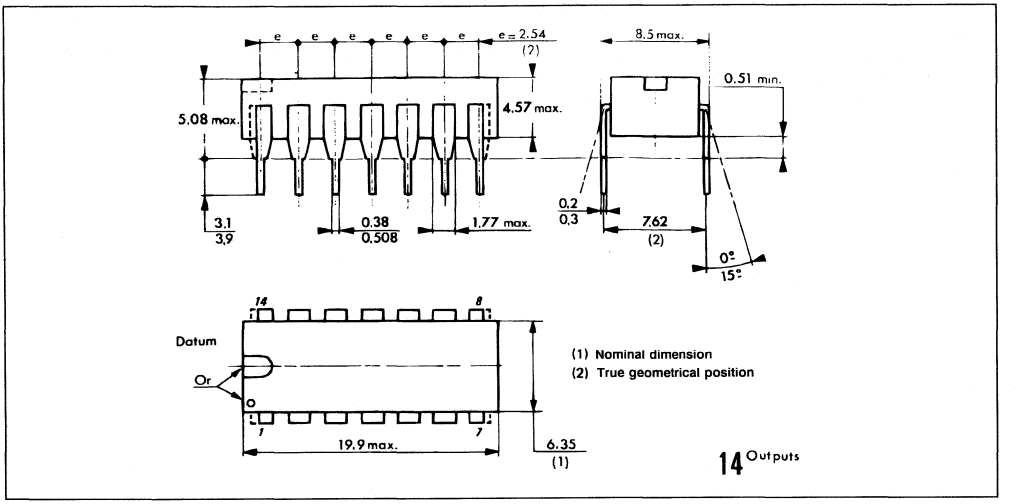
Notes : 1. The offset voltage and offset current which are given are the maximum values required to drive the output down to 400 mV or up to 4 V with R_L = 2.5 KΩ to V_{CC}.
2. The response time which is specified is the interval between the input signal and the instant when the output signal crosses 1.4 V.

ORDER CODES

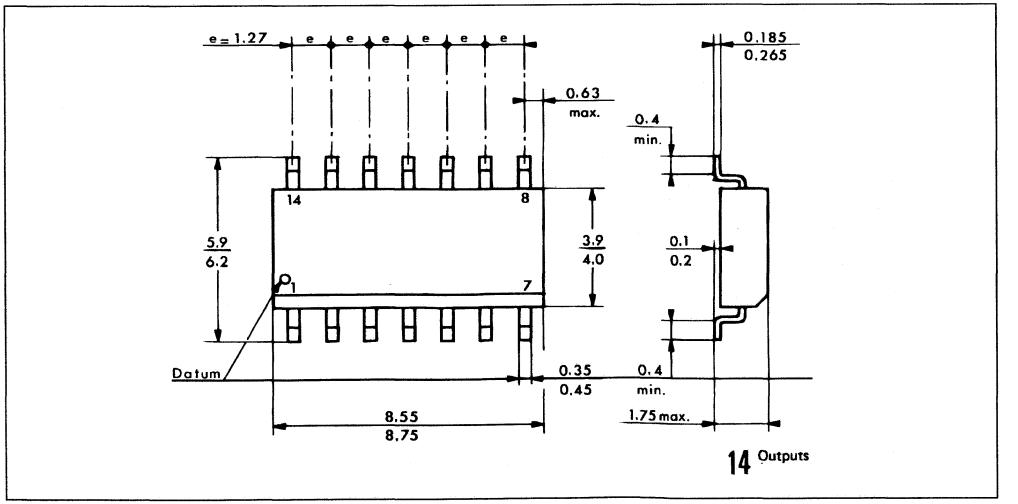
Part Number	Temperature Range	Package		
		N	D	J
TS374	0 to 70	•	•	
TS374I	– 40 to 105	•	•	
TS374M	– 55 to 125			•
Examples : TS374ID				

PACKAGE MECHANICAL DATA

14 PINS - PLASTIC DIP OR CERDIP



14 PINS - PLASTIC MICROPACKAGE SO



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